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A Review on Reversible Quantum Comparator Circuits

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Abstract

This article explores recent advances in reversible logic circuits, particularly focusing on efficient binary comparator designs. Notably, all the methods emphasize key features such as quantum cost, quantum delay, and garbage generation. Together the studies show significant improvements, from a 16.66% reduction in quantum cost to an impressive 63% reduction in quantum delay, achieved through techniques such as logic simplification, prefix clustering, and innovative gate designs. The study underscores the evolving landscape of reversible logic and its applications, including quantum computing and digital comparator optimization. This survey paper reviews various approaches to designing efficient reversible binary comparators. These approaches involve the use of gates such as Peres gates, Feynman gates, reversible NOT gates, controlled V gates, and controlled V+ gates.

Keywords: Quantum computing; Comparator circuit; Quantum cost; Delay; Reversible gate.

Introduction

The field of computing has undergone advancements throughout the years resulting in the exploration of emerging areas, in science and engineering. Researchers worldwide have shown interest in low power computing, quantum computing, nanotechnology and reversible logic. These technologies present opportunities while addressing challenges associated with traditional digital circuits.

One key concern with circuits has been the generation of heat, which not only hampers performance but also leads to information loss. However reversible logic introduces an approach. Reversible circuits exhibit distinct outputs for different input vectors ensuring information preservation and minimising heat dissipation. This characteristic makes them highly appealing for use in quantum computing [1-5], nanotechnology.

The foundation for computing was established by researchers like Rolf Landauer and C.H. Bennett during the early 1960s and 1970s. Landauer showed that the decay of information in computing devices results in heat dissipation measured as KTlog2 joules (where T is the

temperature and K represents Boltzmann's constant). Bennett's work further emphasised the relationship between energy dissipation. Lost information bits. Importantly he highlighted that by making computations reversible energy dissipation can be significantly reduced or even eliminated [1].

Efforts to address power dissipation and performance issues in designing of VLSI have led to increased interest in reversible logic. Traditional CMOS technologies face limitations in terms of size and power consumption, prompting the exploration of alternative computing technologies like reversible logic. Reversible circuits, which adhere to specific constraints such as fan-out and feedback, have been studied extensively. Charles Bennett's work demonstrated that circuitry created from reversible quantum gates exhibit zero power loss.

Reversible computation is made possible through the use of reversible circuits, characterised by their unique design parameters. These parameters include the quantum cost, quantum depth (quantum delay), the number of ancillary inputs (used to maintain reversibility), and the number of garbage outputs (outputs used solely to preserve reversibility).

Extensive research has been devoted to designing reversible gate structures, including arithmetic units such as adders and multipliers. Reversible Arithmetic and Logical Units (ALUs) have also been implemented, contributing to the development of efficient reversible computing systems [6-10]. Various comparator designs have been explored, with a focus on reducing quantum cost and delay[11-16].

This review paper consolidates insights from multiple research papers, encompassing topics such as the principles of reversible logic, the evolution of reversible comparators, and the advantages of low-power and heat-efficient computing. It will also delve into a proposed prefix-based comparator design, which promises substantial reductions in quantum delay, quantum cost, and garbage outputs compared to existing designs. This paper serves as a comprehensive exploration of the burgeoning field of reversible logic and its potential impact on future computing technologies.

Literature Review

- It has been observed in Vudadha, C et al. [10] that this literature review delves into the examination and contrast of types of comparators, with a specific focus on a suggested prefix-based design and its benefits compared to existing designs. Among the existing designs is a tree-based comparator that utilises 2-bit comparator cells. The design we propose relies on generating signals to determine if each pair of bits, in operands A and B is greater or equal. This process consists of a series of stages.

The authors suggest creating g_i and e_i signals, for each pair of operand bits, A_i and B_i. The e_i signal is generated by performing an XOR operation between A_i and the complement of B_i ($e_i = A_i$ xor B_i) while the g_i signal is obtained by performing an operation between A_i and the complement of B_i ($g_i = A_i . B_i'$) . Now let's group together the equal signals. We will use g_i and e_i to represent the equal signals for the ith operand bits as well as for the jth operand bits where j>i

(meaning that the jth bits are more significant than the ith bits). Therefore, we can express the grouped equal signals as follows [10]:

$G_{j,i} = g_j + e_i.g_i$ ..... (1)

$E_{j,i} = e_j.e_i$ ..... (2)

Here 1 is represented by $G_{j,i}$ if $A_j > B_j$ (g_j=1), that is, the MSBs of A are considered greater than the MSBs of B. If the MSBs are same (i.e. $e_i = 1$), then 1 is represented by $G_{j,i}$ if $A_i > B_i$ (i.e. g_i =1). If $A_i <= B_i$ then $G_{j,i}$ is equal to 0 (i.e. g_i =0). When $A_j > B_j$, $E_{j,i}$ (the resultant equal signal) is equal to 1 (i.e. e_j=1) and $A_i = B_i$ (e_i =1), indicating equal operands. The above results are grouped successively to obtain the Final Greater and Equal Signals, G_{N0} and E_{N0}. L_{N0} is obtained by the NOR operation of G_{N0} and E_{N0} as shown below [10] -

$o = \underline{o + o}$

The prefix-based 8-bit comparator Design is shown by the figure

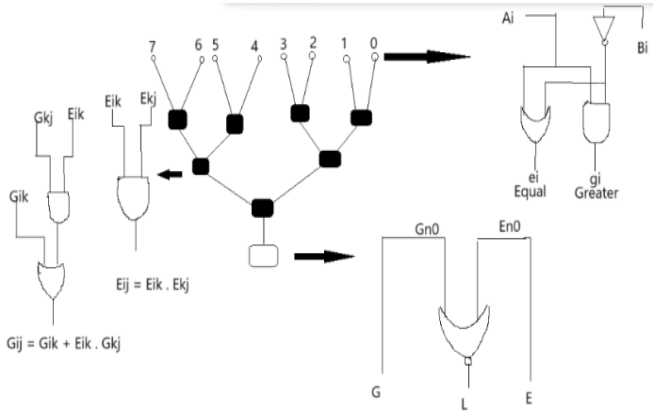

Figure 1: Prefix based 8-bit Comparator Design[10]

The above figure depicts various blocks used in the 8-bit comparator design.[10]

A Peres gate and a NOT gate compute equal and greater signal for 1-bit comparison where the third input of the Peres gate makes 0. This design has a quantum cost and quantum delay of 5 and 5Δ respectively. The figure below shows this

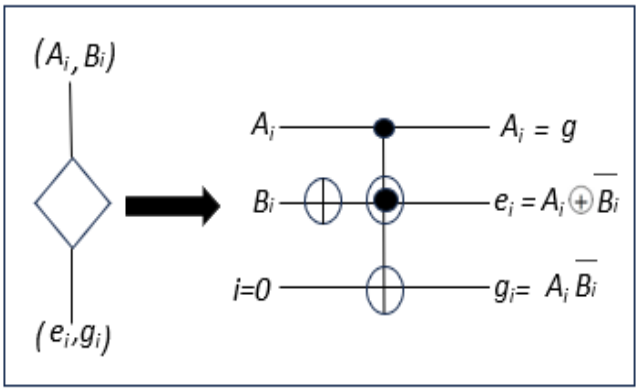

Figure 2: Reversible Computation of Equal and Greater First Stage Signals[10]

The above figure shows the reversible design of computation of equal and greater signal for 1-bit comparison is achieved by using a Peres gate and a NOT gate, with the third input of the Peres gate being made 0.[10]

At the first stage, both greater (g_i) and equal signal (e_i) cannot be equal to 1 at the same time as numbers can't be equal and greater at the same time. Hence, the equation (1) can be written as below [10].

$G_{i+1,i}=g_{i+1}+e_{i+1}\cdot g_i=g_{i+1} \oplus e_{i+1}\cdot g_i$

Similarly, the equations below can be used for grouping in the intermediate stages [10].

Where $i > k > j$

In an intermediate stage, two Peres gates and one CNOT gate are used. To generate group greater signal ($G_{j,i}$) Peres gate is used as per modified form (AB XOR C) of equations (1) and (2). A Peres gate with 0 as its third input can be used for group equal signal (Ei,j) generation. The quantum cost, quantum delay and garbage output of this stage is 9, 5 and 4 respectively. The figure below shows the design of this intermediate stage.

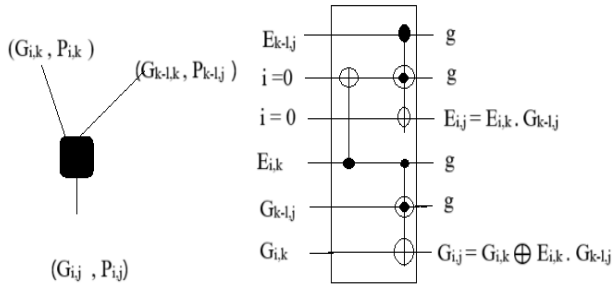

Figure 3: The realization of Black cell used for grouping[10]

Two Peres gates and one CNOT gate consist of the black cell. The grouped greater signal $G_{i,j}$ is generated by one of the two Peres gates and the other Peres gate, with its third input set to constant 0, generates the grouped equal $E_{i,j}$ signal.[10]

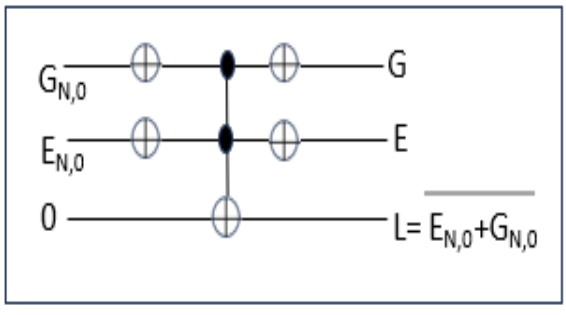

Figure 4: Reversible implementation of output circuit[10]

The final stage is completed with the prefix-based comparator design where a Lesser L signal is generated. This stage is characterized by a quantum cost of 9 and a quantum delay of 7. 0 garbage output is produced by this stage. The circuit for this stage is provided below.

The above figure shows the generation of a Lesser L signal computation is the final stage of the prefix-based comparator.[10]

The proposed design, including an 8-bit and generalised N-bit comparator, is analysed and significant advantages for the proposed approach are revealed. From both serial and tree-based designs, quantum cost, quantum delay, and garbage outputs of this proposed design are reduced, making it optimal in terms of performance. For instance, a 63% reduction in quantum delay, a 21% reduction in quantum cost, and a 16% reduction in garbage outputs are demonstrated by a 64-bit comparator based on the proposed design compared to the existing tree-based design.

In conclusion, the benefits of the proposed prefix-based reversible comparator design are highlighted by this literature review, with its efficiency and superiority across various parameters being emphasised when compared to existing serial and tree-based designs. A promising advancement in reversible comparator technology is shown to be the proposed approach.

- It has been observed in Kalita, G et al. [11] that this research paper examines the development of a GN gate and its applications in comparator circuits. The paper provides an analysis of the GN gate, including its truth table quantum cost (QC) and its versatility as a logic gate for operations like OR, AND, NOT and XOR. A comparator circuit is designed using reversible gates such as Feynman, Toffoli and NOT, as focused on in this paper.

The three input and three output GN gate shown below has inputs A, B and C and outputs P, Q and R. Specifically, A XOR C determines P; A' C XOR B, determines Q; and C is simply R. The GN gate's [11] quantum cost is four, as it is expressed through the use of 2 controlled V gates, 1 controlled V+ gate and 1 controlled-NOT (CNOT) gate. It is also possible for the GN gate to function as a logical OR, AND, NOT and XOR gate based on input combinations. The OR operation is performed when A=B; if B=C, the AND operation is performed. When B=0 and C=1, the NOT operation is executed. The XOR operation is given by the output line.

Here is the block diagram for the GN gate.

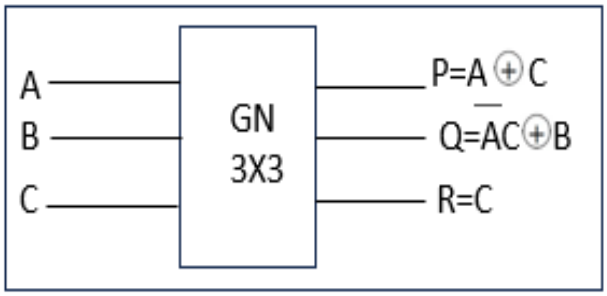

Figure 5: Block Diagram of the reversible GN Gate[11]

The reversible GN gate shown here has three input and three output lines. The three inputs are recognized as A, B, and C. P, Q, and R are recognized as the output lines where P is equal to A XOR C, Q is equal to AC XOR B and R equals C [11].

The research paper underscores the significance of comparator circuits, which are essential for bitwise comparisons and are widely applicable in various domains, including signal processing.

Let the two bits to be compared be A and B. The logic for a single-bit comparator [11] as shown by the authors can be presented as A'B to represent A<B, AB' to represent A>B, and (A XOR B)' to represent A=B. Here the authors used the GN gate to show a 3-single bit comparator. Among these designs, the third comparator circuit is the most suitable one as it showcases the lowest quantum cost. The quantum cost calculates to seven, and it generates a single garbage output; the comparator circuit in Figure (a) contains two GN gates and one NOT gate. Figure (b) uses one GN, one Toffoli, and two NOT gates to demonstrate another single bit comparator. Figure (c) showcases the third comparator circuit with one GN gate, two Feynman gates, and one NOT gate.

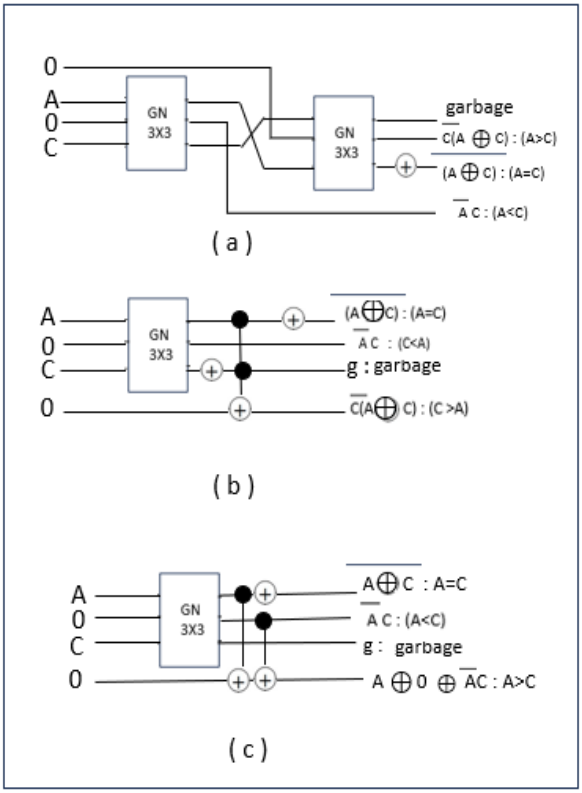

Figure 6: Single Bit Comparator Designs using (a) GN and NOT Gate (b) GN, NOT and Toffoli Gates and (c) GN, Feynman and NOT [11]

The above figure shows two GN and one NOT gate are used by Figure 4(a). One GN, one Toffoli and two NOT gates are used by Figure 4(b) and one GN, two Feynmann and one NOT gate are used by Figure 4(c) [11].

Furthermore, this paper broaches the prospect of extending these designs to accommodate multi-bit comparators. GN gate, NOT gate, Feynman Gates has been used to construct a two-bit comparator [11] as a demonstration. This paper also offers a preliminary circuit to compare two three-bit numbers, hinting at the possibility of creating higher-bit comparators in a cascading fashion. In Figure shown below, as a basic block the 2-bit comparator is used. This design can be extended to construct higher-bit comparators. For instance, the design of a 4-bit comparator from the 3-bit comparator would require 8 NOT gates, 8 GN gates, and 2 Feynman gates.

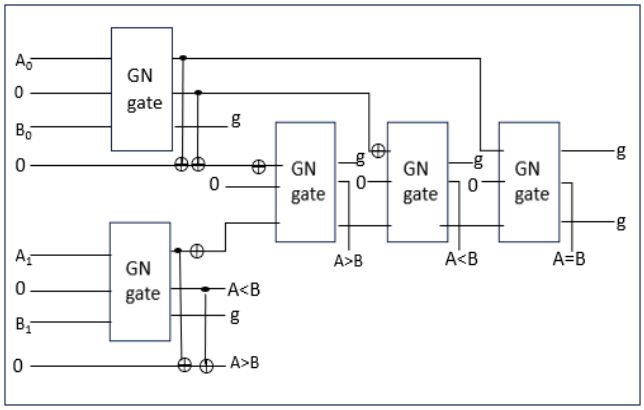

Figure 7: GN, Feynman and NOT gates are used in the design of a two-bit comparator.[11]

The number of Feynman, NOT and GN gates required to design an n-bit comparator (≥2) is determined by using the following expressions:

GN Gate : $+\sum_{=2}(2-1)$

NOT Gate: $(-2)+\sum_{=2}(2-1)$

Feynman Gate: 2

In summary, the research paper offers insights into the development of a reversible GN gate and its utilisation within comparator circuits. The GN gate's unique attributes, including its versatility in logic operations and low quantum cost, make it a compelling choice. The proposed comparator circuits, centred around the GN gate [11], present a reduction in quantum cost compared to alternative designs, rendering them as cost-effective solutions for single-bit comparisons. Additionally, the paper kindles curiosity about the prospects of extending these designs to tackle multi-bit comparators, opening avenues for further research on optimal implementations in higher-bit scenarios.

- It has been observed in Rangaraju, H et al. [12] that a complete study on the design and implementation of quantum comparators employing reversible logic gates is done in this research paper. Quantum comparators serve a significant role in quantum computing, enabling the comparison of quantum states, which is essential for different quantum algorithms and applications. The design and performance analysis of quantum comparators spanning from one-bit to sixty-four-bit are examined by the study, providing insights into their quantum cost, constant inputs, and garbage outputs. The proposed circuit is divided into two parts, the first one being the Input circuit and the second one being a one-bit reversible binary comparator.

The study paper begins by introducing the design of the input circuit, which takes the Most Significant Bit (MSB) as input to the whole comparator circuit. Three inputs (An, Bn, and logical low) are included in this input circuit, and its outputs are composed of A Equal to B (AEB), A Greater than B (AGB), and A Less than B (ALB). A combination of a PG (Peres gate), two CNOT (Controlled-NOT), and a NOT gate is employed by the authors to form the input circuit, with its capacity to operate as a one-bit comparator being stressed. The NOT gate is connected to

input B, which results in B'. The PG gate has A, B', and Logic Low (0) connected to it. The first input of the $CNOT_1$ gate is connected to one output of the PG gate, and the second input of $CNOT_1$ is connected to Logic High (1). Another output of the PG gate is given along with an output of the $CNOT_1$ gate as input to the $CNOT_2$ gate.

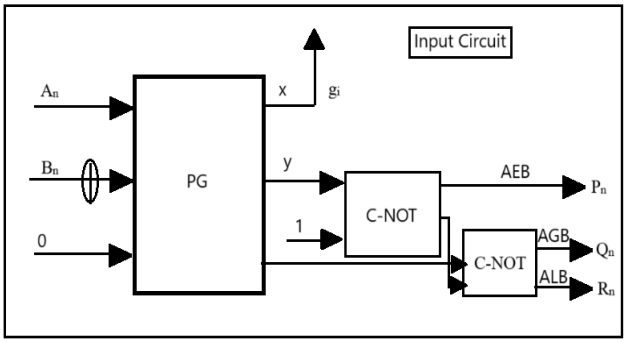

Figure 8: Input Circuit of the Reversible Binary Comparator[12]

The above figure shows the binary comparator is used by the input circuit using reversible logic.[12]

The one bit comparator cell, which consists of three NOT gates, three PG gates and four CNOT gates, is moved onto after that by us. In the circuit, five inputs and three outputs are present. The inputs are P_n (AEB), Q_n (AGB), R_n (ALB), A_{n-1}, and B_{n-1} and the outputs are Q_{n-1} (AGB), P_{n-1} (AEB), and R_{n-1} (ALB). The circuit of this comparator cell is shown below -

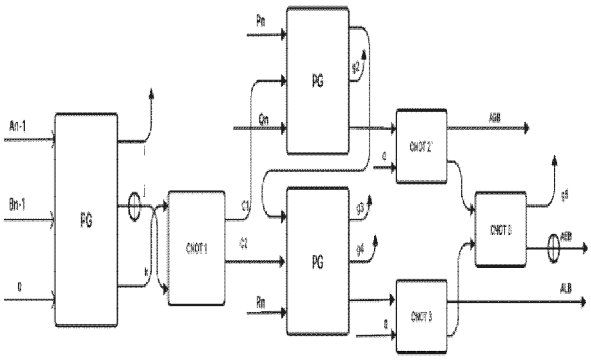

Figure 9: One-Bit Reversible Binary Comparator[12]

The figure shows three PG and four CNOT gates consisting of a one-bit reversible binary comparator. It is equipped with five inputs viz., P_n (AEB), Q_n (AGB), R_n (ALB), A_{n-1} and B_{n-1} and three outputs Q_{n-1} i.e., AGB, P_{n-1} i.e., AEB and R_{n-1}i.e., ALB are shown in the figure. [12]

Building upon this foundation the study delves into the exploration of designing comparators with multiple bits. Two-bit, three-bit, four-bit, eight-bit, sixteen bit and thirty-two-bit comparators are included in these. To create these designs the one-bit comparators are interconnected in a particular manner. The quantum cost, constant inputs and garbage outputs for each of these multi bit comparators are meticulously presented by the researchers.

Additionally, the authors provide an analysis of performance where they summarise the quantum cost, constant inputs and garbage outputs for eight-bit, sixteen bits, thirty-two bit and sixty-four bit comparators. A comparison is made with existing methodologies to demonstrate the efficiency and scalability of the proposed design.

The below formula is used to find out the QC for N-bit reversible binary comparator.

- QC = QC of input circuit + ((N-1)*QC of 1-bit Comparator cell) = 6 + (N-1) x 16 [12]

The below formula is used to find out the CI for N-bit reversible binary comparator.

- CI = CIs of input circuit + ((N-1) * Cis of 1-bit Comparator cell) = 2 + (N-1) x 3 [12]

The below formula is used to find out the GO for N-bit reversible binary comparator.

- GOs=GOs of input circuit + ((N-1)*GOs of 1-bit comparator cell) = 1 + (N-1) x 5 [12]

Table 1: Comparison of Performance of Various Bit Comparator[12]

Parameter	1-Bit	2-Bit	3-Bit	8-Bit	16-Bit	32-Bit	64-Bit
Quantum Cost (QC)	16	22	38	118	246	502	1014
Constant Input (CI)	3	6	8	23	47	95	191
Garbage Output (GO)	5	6	11	36	76	156	316

To sum up, this research study thoroughly investigates the design of quantum comparator circuits covering comparators ranging from one bit to sixty-four bits. The systematic design approach and in-depth performance analysis provide insights for researchers and professionals in the field of quantum computing. The proposed designs present solutions for comparing quantum states with potential applications in quantum algorithms and processing quantum information. Future research can focus on implementations and enhancements of these quantum comparators to increase their applicability, in real world scenarios.

- It has been observed in Maity, H [13] that a method for improving the efficiency of a quantum comparator circuit operating on two qubits is developed in this review. The authors suggest a design and practical implementation of this circuit using reversible gates. To verify its functionality, they conduct experiments with the IBM Qiskit simulator. The paper offers a description of the circuits structure the logic functions utilised and its performance evaluation based on Quantum Cost (QC) Gate Count (GC) and delay metrics.

A 2-bit comparator circuit, which has two input terminals, A1, A0 and B1, B0 and three output terminals X, Y, Z, [4] is introduced at the beginning of the paper. The truth table for this circuit is provided, and from it, the logic functions for X, Y, and Z are derived. The key logic functions identified are as follows:

Table 2: Truth Table of 2-Bit Comparator[13]

A1	A0	B1	B0	X A<B	Y A=B	Z A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

->X = [(A1⊙B1)A0′B0 + A1′B1]

-> Y = (A0⊙B0)(A1⊙B1)

-> Z = A1B1' + B0'(A0B1' + A0A1) = X⊙Y [13]

They describe this innovative technique as applicable to N - bit comparator circuits, offering circuit complexity reduction.

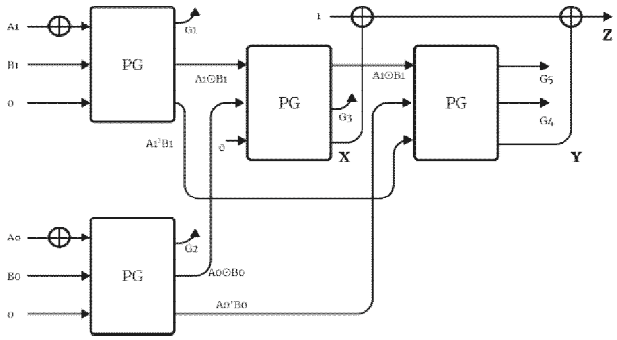

Figure 10: The reversible two qubit Q-CC with QC-18, GO-5, and delay-5.[13]

The reversible optimized circuit using four PG, two FG and two reversible NOT gates is shown by the figure.[14-16]

The authors proceed to implement the above-simplified logic functions in a quantum circuit. They introduce a reversible optimised circuit using 4 Peres gates (PG), 2 Feynman gates (FG), and 2 reversible NOT gates.

The key contributions of this research are summarized in the conclusion of the paper. The authors highlight the designing and implementation of a 2-qubit Q-CC with a notable improvement in Quantum Cost (QC), Gate Count (GC), and delay over previous results. The proposed circuit, utilising a combination of Peres gates, Feynman gates, and reversible NOT gates, exhibits a QC of 18, GC of 8, and a delay of 5. Importantly, these figures represent an enhancement of 16.66%, 37.5%, and 20% in QC, delay, and GC, respectively, in comparison to previously reported results. [13] This innovative work showcases the potential for significant advances in quantum circuit optimization and resource efficiency.

Table 3: Comparison Table of the Literature Reviews

	QC	GO	Delay	No. of Gates
Ref. [10]	28	6	7	12
Ref. [11]	24	6	7	12
Ref. [12]	22	6	9	10
Ref. [13]	18	8	5	8

Applications of Reversible Comparator

A type of logic circuit, known as a reversible comparator, can be used to compare two numbers and outputs indicating their magnitude such as whether they are equal, greater than or less than each other can be provided. Unlike comparators, reversible comparators do not lose any information. Dissipate energy during the comparison process. Applications in emerging technologies like quantum computing, optical computing, DNA computing and low power CMOS design are found by these specialized circuits.

Reversible comparators have uses-

- **Quantum computing:** In quantum algorithms involving comparison operations like sorting, searching, encryption reversible comparators play a role. They are also used to create error correction codes for identifying and fixing errors in quantum states.[9]
- **Optical computing:** Reversible comparators can be employed to design devices of performing comparison operations using light signals.[14] Optical comparators offer advantages such as speed, parallelism and low power consumption.[5]
- **DNA computing:** By utilising comparators it is possible to develop DNA based systems that perform comparison operations through interactions. DNA comparators have the potential for features like storage capacity, biocompatibility and self-assembly.[6]

Overall reversible comparators find applications in cutting edge technologies where preserving information integrity and minimising energy dissipation are factors.

Reversible comparators can be used in low power CMOS design to create circuits that perform comparison tasks while minimising energy consumption. The utilisation of low power competitors can bring advantages such as reduced heat generation, longer battery life and environmental friendliness, among others.[16]

Conclusion

In summary the combined results from the four research articles demonstrate advancements in the design of quantum comparator circuits. The first study presents a comparator design that outperforms previous serial and tree based systems in terms of efficiency and superiority representing a notable breakthrough in the field. The second research introduces a GN gate within comparator circuits offering a cost solution for single bit comparisons and raising questions about its applicability in multi bit scenarios. The third paper thoroughly investigates quantum comparators ranging from one bit to sixty four bit designs emphasising their importance in quantum computing and providing avenues for implementation and further development. The fourth article discusses an implementation of Q CC with improvements in Quantum Cost, Gate Count and latency pointing towards progress in optimising quantum circuits and resource efficiency. Collectively these findings open doors to possibilities and advancements, in the realm of quantum comparator technology.

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