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INTRODUCTION TO INTEL CHIPSET ARCHITECTURE

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ABSTRACT

This chapter gives an overview about Intel's next generation chipset and basic blocks of the chipset architecture. The best way to define chipset is as a set of chips that provides the interfaces between all of the PC's subsystems. It provides the buses and electronics to allow the CPU, memory and input/output devices to interact. Earlier Intel used the name "Triton" for its chipsets. It also used the name PCIset for PCI-based chipsets.

KEYWORDS: Chipset Architecture, PCI, MCH / GMCH, ICH, Unified Shader Architecture.

INTRODUCTION

The generalized layout of chipset is shown in figure 1. The architecture is consists the CPU, GMCH, IO controller, Memory, External GPU etc.

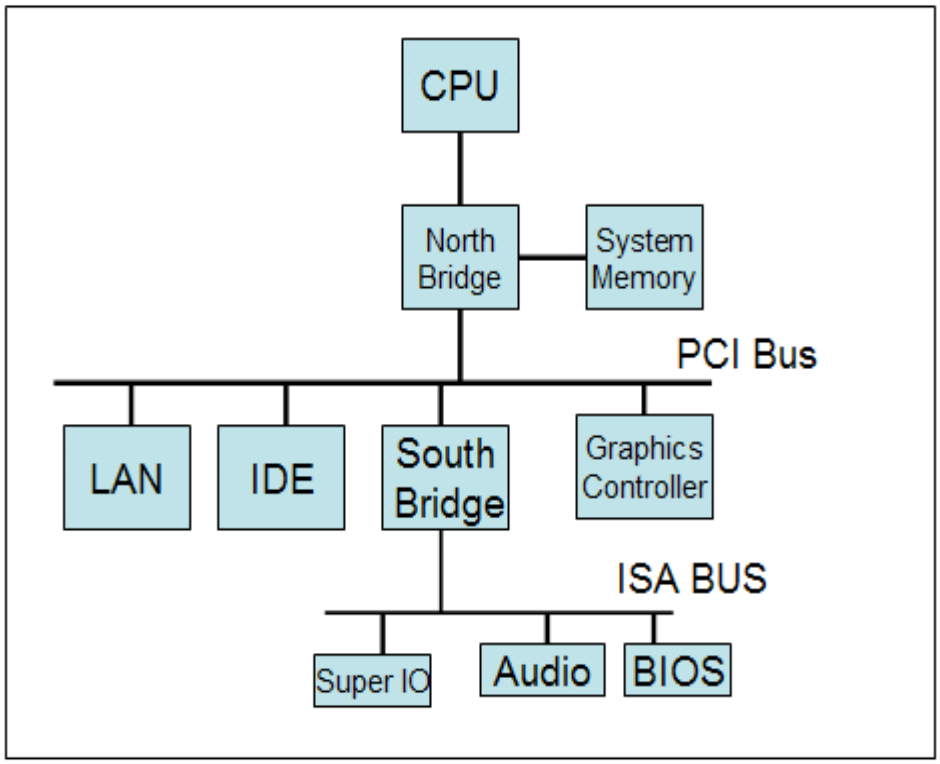

Figure 1.Chipset Layout

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The chipset architecture is divided in three main parts

- CPU
- Northbridge.(MCH / GMCH)
- Southbridge (ICH)

The orientations of these blocks are shown in the figure 2 shown below. The Northbridge and the Southbridge these two "bridges" connect the CPU to other parts of the computer. The Northbridge links the CPU to very high-speed devices, especially main memory and graphics controllers, and the Southbridge connects to lower-speed peripheral buses (such as PCI or ISA). In many modern chipsets, the Southbridge actually contains some on-chip integrated peripherals, such as Ethernet, USB, and audio devices.

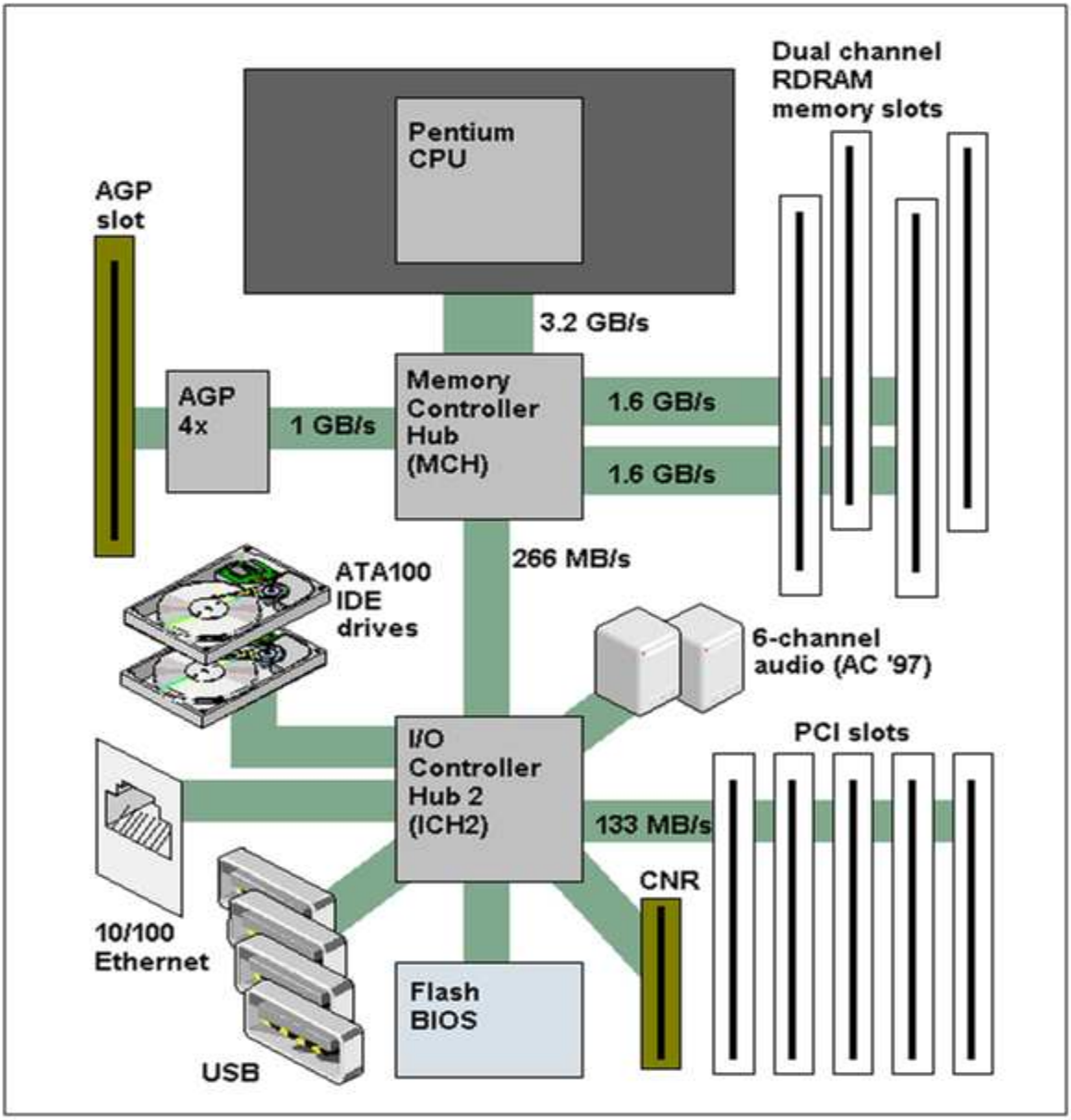

Figure 2.Chipset Architecture

A chipset is typically intended to work with a particular family of microprocessors. Since it controls interchanges between the processor and external devices, the chipset assumes a pivotal part in deciding system performance.

NORTHBRIDGE (MCH / GMCH)

The Northbridge is also known as MCH/GMCH. This part controls functionality of DDRAM and the

AGP slots. The most important function of this block is to support the graphic functionality.

The figure 3 below shows that the overall system architecture remains largely unchanged, a great number of graphics improvements have been made to overcome the benefits once provided by zone rendering. The list includes a larger graphics aperture size, an increase in core clock frequency.

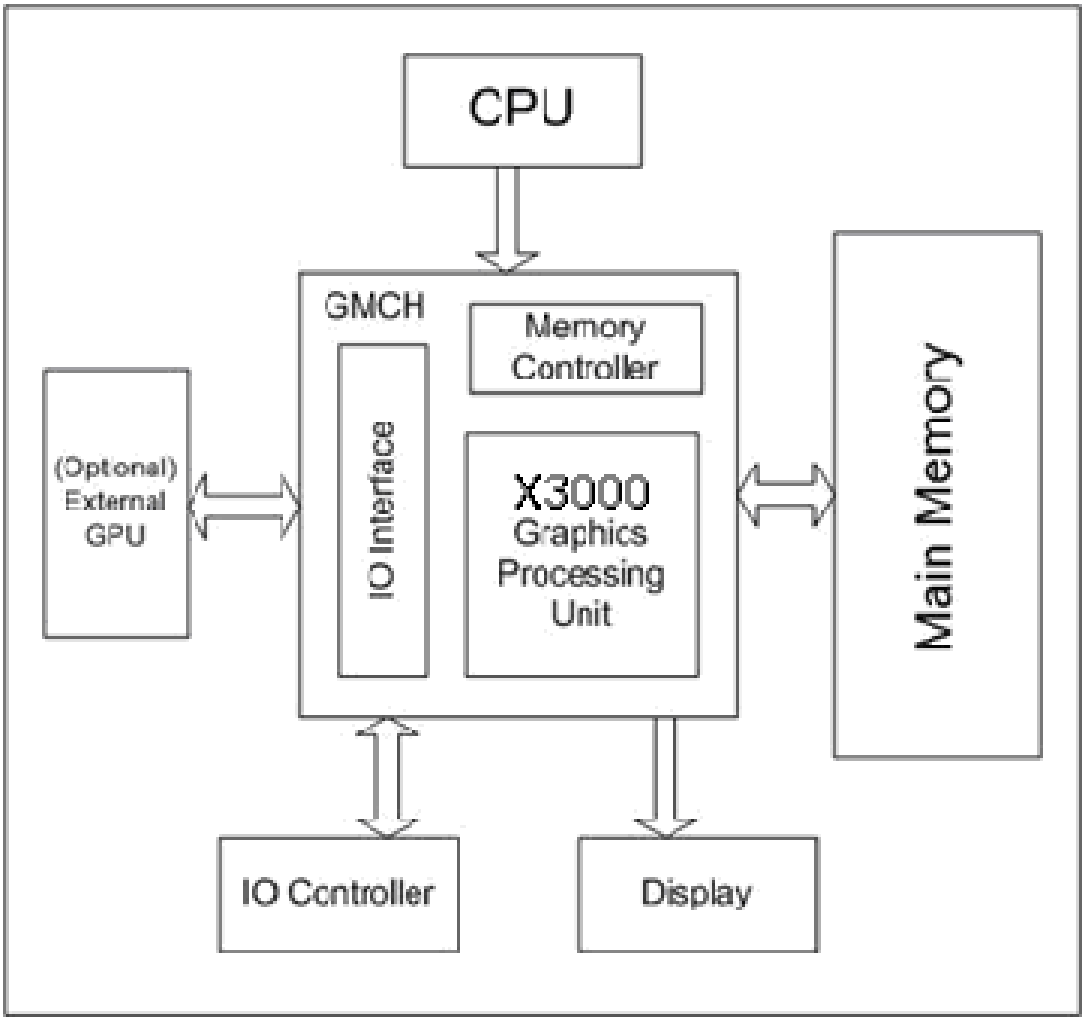

Figure 3.layout including GMCH, ICH and main memory

The advantage of unified shader architecture is that the measure of handling power connected to vertices and pixels can be dynamically adjusted by the requirements of a specific edge of an application. Architectures lacking bound together shaders may leave vertex shaders sit still while the pixel shaders are over-burden on outlines that contain extensive triangles. Then again, outlines that contain numerous little triangles tend to bring about sit out of gear pixels shaders while the vertex shaders are over-burden. The brought together approach doles out execution units to vertices or pixels as required and therefore limits sit out of gear execution units and gives a superior value execution proportion in light of the fact that hypothetically the end client abstains from paying for silicon that is sit out of gear a great part of the time. The figure 4 demonstrates the GMCH pipelined design.

The path Command Stream (CS), Vertex Shader (VS), Clip Unit (CU), Strips / Fan unit, Windower is collectively named as 3-D pipeline.

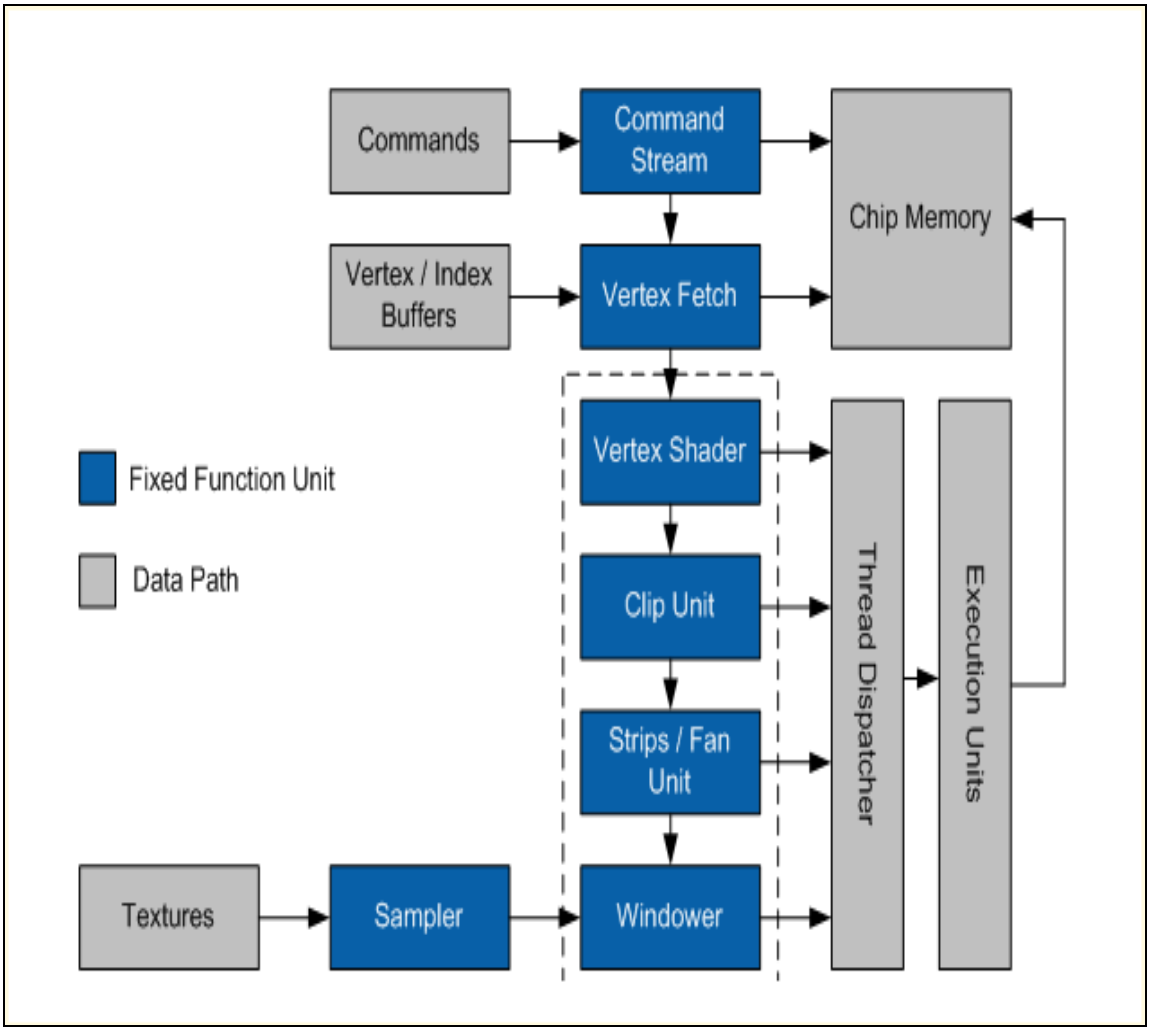

Figure 4.GMCH pipelined architecture

BLOCKS DESCRIPTION USED IN GMCH ARCHITECTURE

COMMAND STREAM

This stage is responsible for dealing with the 3D pipeline and passing orders down the 3D pipeline. Also it peruses "steady information" from memory cushions and places it into Chip Memory. The Command Stream arranges is shared between the 3D and Media pipelines.

VERTEX FETCH

This stage is responsible for reading vertex data from Chip Memory, reformatting it, and writing the results into new vertex entries in the Chip Memory.

VERTEX SHADER

This stage is responsible for dealing with the 3D pipeline and passing orders down the 3D pipeline. Also it peruses "steady information" from memory cushions and places it into Chip Memory. The Command Stream arranges is shared between the 3D and Media pipelines:

- Vertex transformations
- Vertex Lighting
- Point size

CLIP UNIT

The functions of this stage are performed in two parts. Initially the fixed function portion of the Clip Unit is responsible for categorizing the input primitive into one of three states:

- TRIVIAL_ACCEPT – the primitive falls completely within the view frustum and is simply passed to the next stage of the 3D pipeline
- TRIVIAL_REJECT – the primitive is not visible within the view frustum and is removed from the 3D pipeline
- MUST_CLIP – at least one edge of the primitive straddles a view frustum boundary so a kernel program must be dispatched to handle 3D clipping, i.e. computing the new vertices that intersect the view frustum.

In addition to computing the new vertices of a clipped primitive, the CLIP thread is also used to handle wireframe triangles.

STRIP/FAN UNIT

The elements of this stage are performed in two sections. At first the settled capacity part of the Strip/Fan Unit is in charge of applying the viewport change to put the approaching crude into screen space Culling the approaching crude on the off chance that it is back confronting This stage at that point performs crude setup by means of utilization of produced setup strings to do coefficient calculation and vertex characteristic insertion.

WINDOWER/MASKER

The functions of this stage are performed in two parts. Initially the fixed function portion of the Windower/Masker Unit performs primitive rasterization. It then spawns a pixel shader thread to shade the primitive's pixels.

The GMCH as the name suggests contains the graphics and memory controllers and the proper break down of components is:

- System Bus Interface.
- System Memory Interface.
- Display Interface.
- Display Cash Interface
- Digital TV-Out
- Clock Signal
- Hub Interface

The figure 5 shows the GMCH architecture. This figure gives an idea where these units are connected to the outer world.

As different display devices are available in the market the output signal formats different eg. Analog/ Digital.

SOUTHBRIDGE (ICH)

The Southbridge is also known as the ICH (IO control hub) depending on its functionality. AS the name indicate this block deals with the Input Output devisees. The first version of the ICH was released in June 1999 along with the Intel 810 Northbridge. The Hub Interface is nothing but a point-to-point connection between different components on the motherboard. Another design decision is to substitute the rigid North-South axis on the motherboard with a star structure. Note that, along with the ICH, Intel evolved other uses of the "Hub" terminology. Thus, the Northbridge became the MCH or if it had integrated graphics the Graphics and Memory Controller Hub (GMCH).

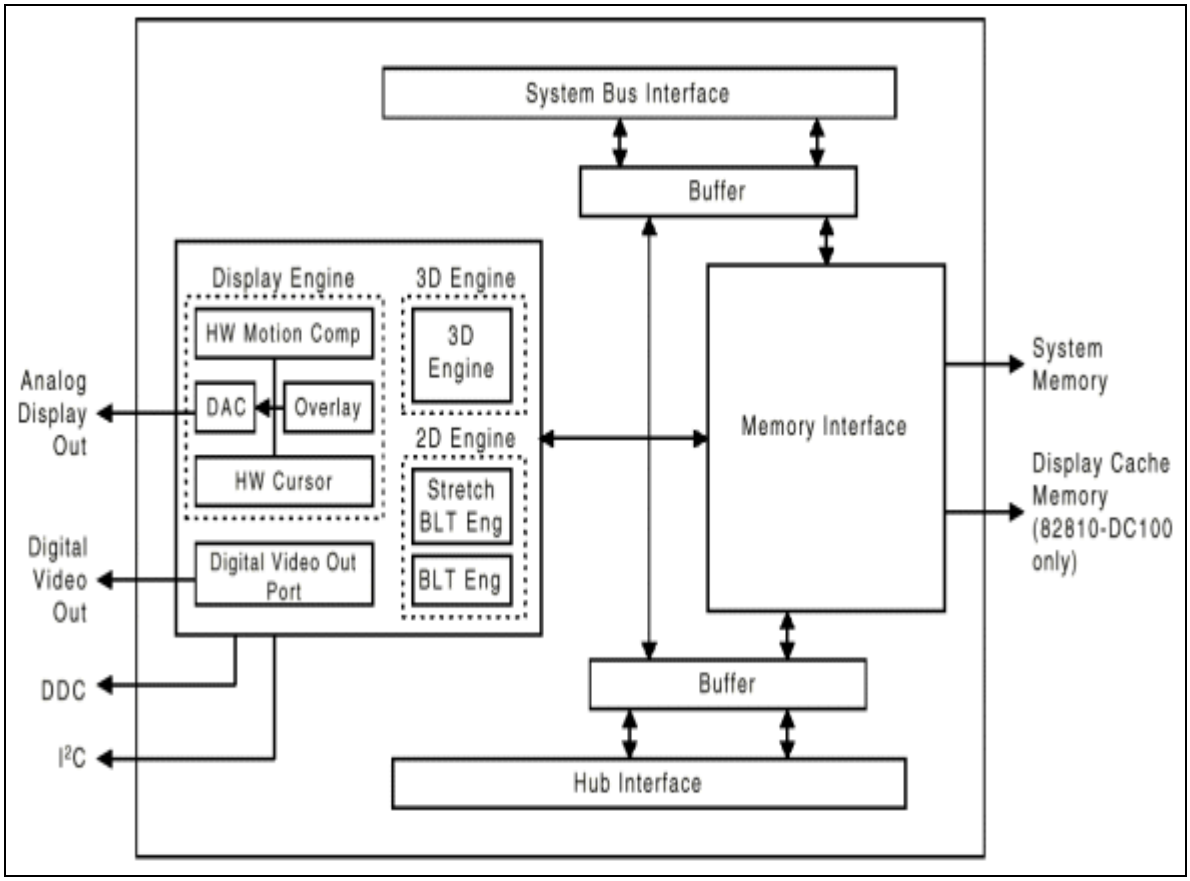

Figure 5.Architecture of GMCH

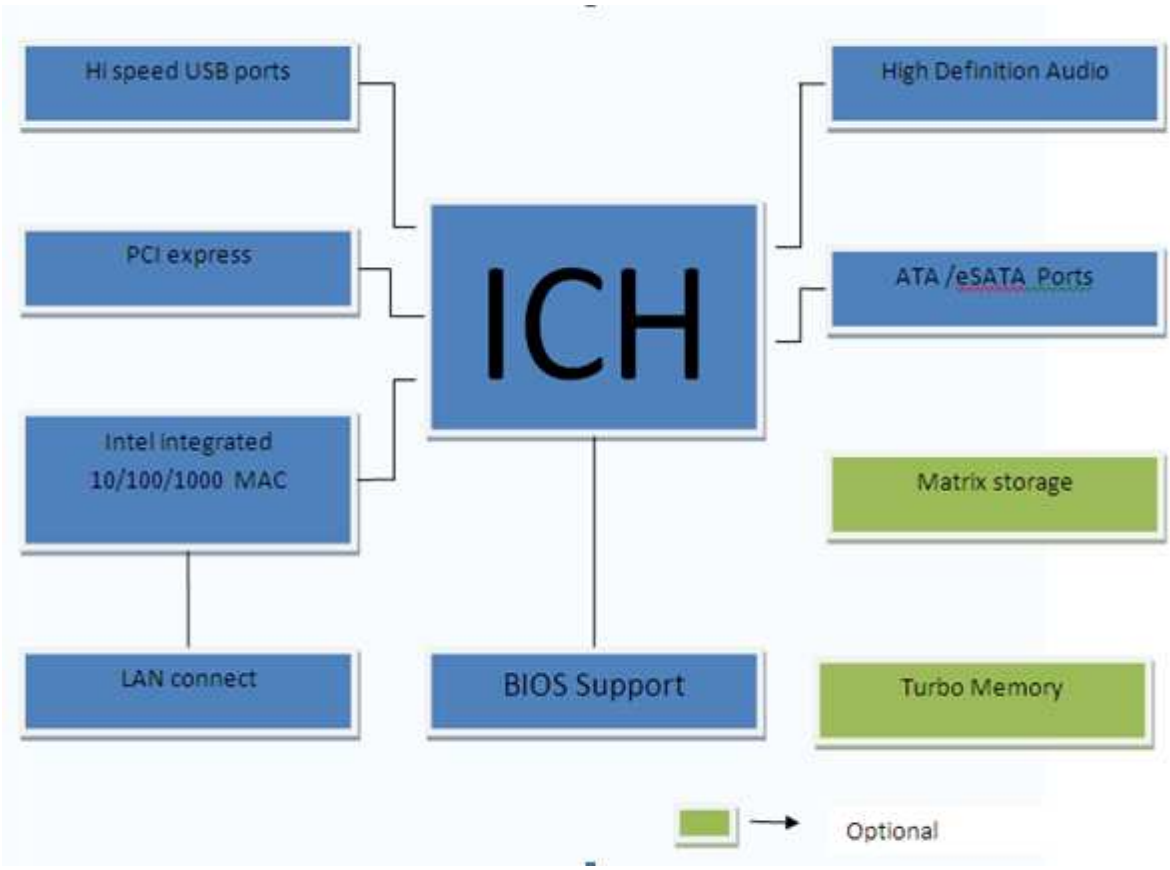

Figure 6.Block Diagram of Input/ Output Controller Hub (ICH)

This hub the Input/ Output Controller Hub (ICH) is a profoundly coordinated multifunctional I/O Controller Hub that utilizes the Intel Accelerated Hub Architecture (AHA) to make an immediate association from the designs and memory to the incorporated AC97 controller, the IDE controllers, double USB ports, and PCI include cards.

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